

LOW-INPUT VOLTAGE-MODE SYNCHRONOUS BUCK CONTROLLER

FEATURES

- Operating Input Voltage 2.25 V to 5.5 V
- Output Voltage as Low as 0.7 V
- 1% Internal 0.7 V Reference
- Predictive Gate Drive™ N-Channel MOSFET Drivers for Higher Efficiency
- Externally Adjustable Soft-Start and Overcurrent Limit
- Source-Only Current or Source/Sink Current
- Versions for Starting Into V_{OUT} Pre-Bias
- 10-Lead MSOP PowerPad™ Package for Higher Performance
- Thermal Shutdown
- Internal Bootstrap Diode
- Fixed-Frequency, Voltage-Mode Control
 - TPS40000/1/4 300-kHz
 - TPS40002/3/5 600-kHz

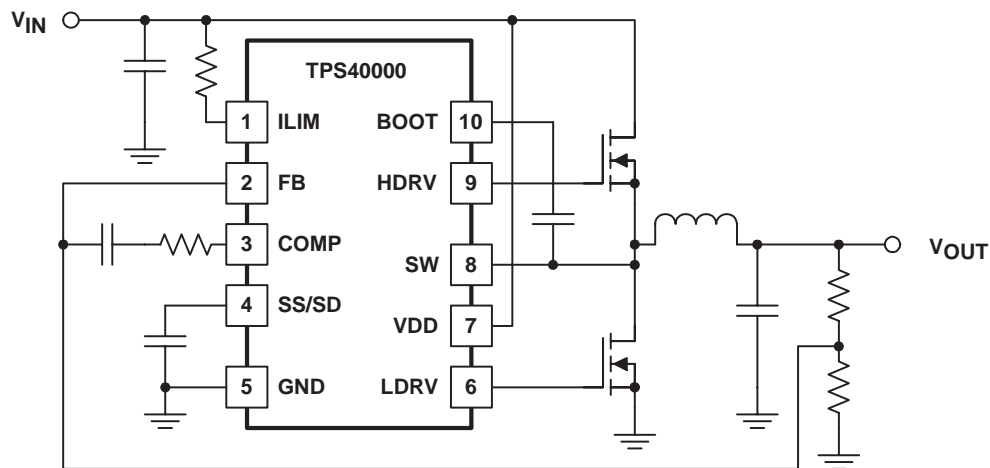
APPLICATIONS

- Networking Equipment
- Telecom Equipment
- Base Stations
- Servers
- DSP Power
- Power Modules

DESCRIPTION

The TPS4000x are controllers for low-voltage, non-isolated synchronous buck regulators. These controllers drive an N-channel MOSFET for the primary buck switch, and an N-channel MOSFET for the synchronous rectifier switch, thereby achieving very high-efficiency power conversion. In addition, the device controls the delays from main switch off to rectifier turn-on and from rectifier turn-off to main switch turn-on in such a way as to minimize diode losses (both conduction and recovery) in the synchronous rectifier with TI's proprietary Predictive Gate Drive™ technology. The reduction in these losses is significant and increases efficiency. For a given converter power level, smaller FETs can be used, or heat sinking can be reduced or even eliminated.

SIMPLIFIED APPLICATION DIAGRAM



UDG-01141

PowerPAD™ and Predictive Gate Drive™ are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TPS40000, TPS40001
TPS40002, TPS40003
TPS40004, TPS40005

SLUS507D – JANUARY 2002 – REVISED NOVEMBER 2005

DESCRIPTION (continued)

The current-limit threshold is adjustable with a single resistor connected to the device. The TPS4000x controllers implement a closed-loop soft start function. Startup ramp time is set by a single external capacitor connected to the SS/SD pin. The SS/SD pin is also used for shutdown.

ORDERING INFORMATION

T _A	FREQUENCY	PACKAGED DEVICES MSOP ⁽²⁾ (DGQ)		
		APPLICATION		
		SOURCE ONLY	SOURCE/SINK WITH PREBIAS ⁽³⁾	SOURCE/SINK ⁽³⁾
-40°C to 85°C	300 kHz	TPS40000DGQ	TPS40001DGQ	TPS40004DGQ
	600 kHz	TPS40002DGQ	TPS40003DGQ	TPS40005DGQ

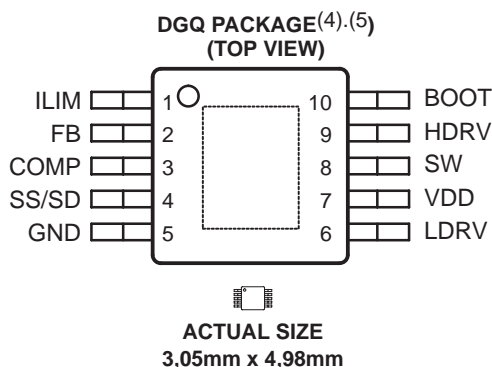
- (2) The DGQ package is available taped and reeled. Add R suffix to device type (e.g. TPS40000DGQR) to order quantities of 2,500 devices per reel and 80 units per tube.
- (3) See Application Information section, p. 8.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

	TPS4000x	UNIT
Input voltage range, V _{IN}	BOOT	V _{SW} + 6.5
	COMP, FB, ILIM, SS/SD	-0.3 to 6
	SW	-0.7 to 10.5
	SW _T (SW transient < 50 ns)	-2.5
	VDD	6
Operating junction temperature range, T _J	-40 to 150	°C
Storage temperature, T _{stg}	-55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



- (4) See technical brief SLMA002 for PCB guidelines for PowerPAD packages.
- (5) PowerPAD™ heat slug can be connected to GND (pin 5).

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{DD} = 5.0\text{ V}$, all parameters measured at zero power dissipation (unless otherwise noted)

input supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input voltage range		2.25		5.5	V
V_{HGATE}	High-side gate voltage	$V_{BOOT} - V_{SW}$			5.5	
I_{DD}	Shutdown current	$SS/SD = 0\text{ V}$, Outputs off		0.25	0.45	mA
	Quiescent current	$FB = 0.8\text{ V}$		1.4	2.0	
	Switching current	No load at HDRV/LDRV		1.5	4.0	
$UVLO$	Minimum on-voltage		1.95	2.05	2.15	V
	Hysteresis		80	140	200	mV

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	$2.25\text{ V} \leq V_{DD} \leq 5.00\text{ V}$	250	300	350	kHz
			500	600	700	
V_{RAMP}	Ramp voltage	$V_{PEAK} - V_{VALLEY}$	0.80	0.93	1.07	V
	Ramp valley voltage		0.24	0.31	0.41	

PWM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum duty cycle(2)	TPS40000 TPS40001 TPS40004	$FB = 0\text{ V}$, $V_{DD} = 3.3\text{ V}$	87%	94%	97%	
	TPS40002 TPS40003 TPS40005		83%	93%	97%	
Minimum duty cycle					0%	

error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	FB input voltage	Line, Temperature	0.689	0.700	0.711	V
		$T_A = 25^\circ\text{C}$	0.693	0.700	0.707	
	FB input bias current			30	130	nA
V_{OH}	High-level output voltage	$FB = 0\text{ V}$, $I_{OH} = 0.5\text{ mA}$	2.0	2.5		V
V_{OL}	Low-level output voltage	$FB = V_{DD}$, $I_{OL} = 0.5\text{ mA}$		0.08	0.15	
I_{OH}	Output source current	$COMP = 0.7\text{ V}$, $FB = GND$	2	6		mA
I_{OL}	Output sink current	$COMP = 0.7\text{ V}$, $FB = V_{DD}$	3	8		
GBW	Gain bandwidth(1)		5	10		MHz
A_{OL}	Open loop gain		55	85		dB

(1) Ensured by design. Not production tested.

(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{DD} = 5.0\text{ V}$, all parameters measured at zero power dissipation (unless otherwise noted)

current limit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SINK}	ILIM sink current	$V_{DD} = 5\text{ V}$	11	15	19	μA
		$V_{DD} = 2.25\text{ V}$	9.5	13.0	16.5	
V _{OS}	Offset voltage SW vs ILIM ⁽¹⁾	$2.25\text{ V} \leq V_{DD} \leq 5.00$	-20	0	20	mV
V _{ILIM}	Input voltage range		2		V _{DD}	V
t _{ON}	Minimum HDRV pulse time in overcurrent	$V_{DD} = 3.3\text{ V}$		200	300	ns
	SW leading edge blanking pulse in overcurrent detection			100		ns
t _{SS}	Soft-start capacitor cycles as fault timer ⁽¹⁾			6		

rectifier zero current comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SW}	Sense voltage to turn off rectifier	TPS40000 TPS40002 LDRV output OFF	-15	-7	-2	mV
	SW leading edge blanking pulse in zero current detection			75		ns

predictive delay

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SWP}	Sense threshold to modulate delay time			-350		mV
T _{LDHD}	Maximum delay modulation range time	LDRV OFF – to – HDRV ON	50	75	100	ns
	Predictive counter delay time per bit	LDRV OFF – to – HDRV ON	3.0	4.5	6.2	ns
T _{HDL}	Maximum delay modulation range	HDRV OFF – to – LDRV ON	40	65	90	ns
	Predictive counter delay time per bit	HDRV OFF – to – LDRV ON	2.4	4.0	5.6	ns

shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SD}	Shutdown threshold voltage	Outputs OFF	0.09	0.13	0.205	V
V _{EN}	Device active threshold voltage		0.14	0.17	0.235	V

soft start

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SS}	Soft-start source current	Outputs OFF	2.0	3.7	5.4	μA
V _{SS}	Soft-start clamp voltage		1.1	1.5	1.9	V

bootstrap

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{BOOT}	Bootstrap switch resistance	$V_{DD} = 3.3\text{ V}$		50	100	Ω
		$V_{DD} = 5\text{ V}$		35	70	

(1) Ensured by design. Not production tested.

(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range, $T_A = -40^\circ\text{C}$ to 85°C , $V_{DD} = 5.0\text{ V}$, all parameters measured at zero power dissipation (unless otherwise noted)

output driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{HDHI}	HDRV pull-up resistance	$V_{BOOT} - V_{SW} = 3.3\text{ V}$, $I_{SOURCE} = -100\text{ mA}$		3	5.5	Ω
R _{HDLO}	HDRV pull-down resistance	$V_{BOOT} - V_{SW} = 3.3\text{ V}$, $I_{SINK} = 100\text{ mA}$		1.5	3	
R _{LDHI}	LDRV pull-up resistance	$V_{DD} = 3.3\text{ V}$, $I_{SOURCE} = -100\text{ mA}$		3	5.5	
R _{LDLO}	LDRV pull-down resistance	$V_{DD} = 3.3\text{ V}$, $I_{SINK} = 100\text{ mA}$		1.0	2.0	
t _{RISE}	LDRV rise time	$C_{LOAD} = 1\text{ nF}$		15	35	ns
t _{FALL}	LDRV fall time			10	25	
	HDRV rise time			15	35	
	HDRV fall time			10	25	

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{SD}	Shutdown temperature ⁽¹⁾			165		°C
	Hysteresis ⁽¹⁾			15		

sw node

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SW}	Leakage current in shutdown ⁽¹⁾			15		μA

(1) Ensured by design. Not production tested.

(2) At V_{DD} input voltage of 2.25 V, derate the maximum duty cycle by 3%.

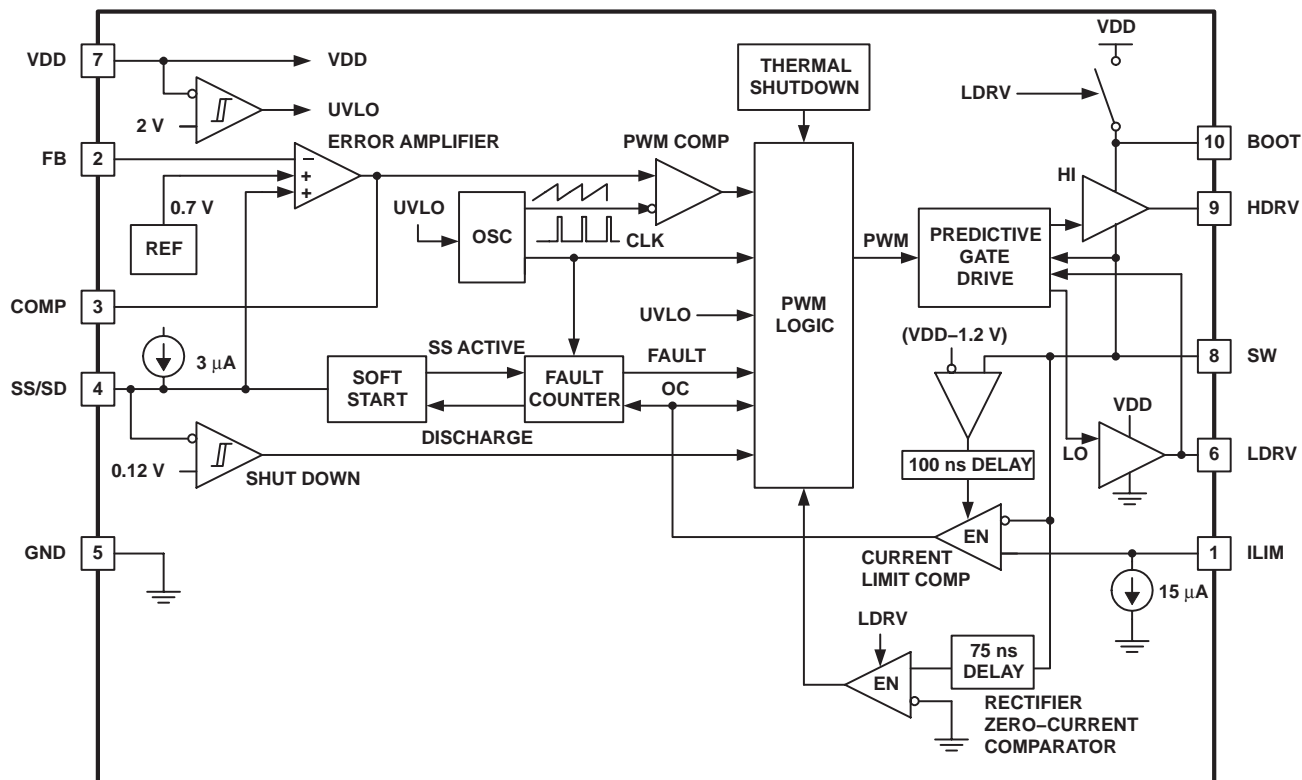
TPS40000, TPS40001
TPS40002, TPS40003
TPS40004, TPS40005

SLUS507D – JANUARY 2002 – REVISED NOVEMBER 2005

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	10	O	Provides a bootstrapped supply for the topside MOSFET driver, enabling the gate of the topside MOSFET to be driven above the input supply rail
COMP	3	O	Output of the error amplifier
FB	2	I	Inverting input of the error amplifier. In normal operation the voltage at this pin is the internal reference level of 700 mV.
GND	5	–	Power supply return for the device. The power stage ground return on the board requires a separate path from other sensitive signal ground returns.
HDRV	9	O	This is the gate drive output for the topside N-channel MOSFET. HDRV is bootstrapped to near $2 \times V_{DD}$ for good enhancement of the topside MOSFET.
ILIM	1	I	A resistor is connected between this pin and VDD to set up the over current threshold voltage. A 15- μ A current sink at the pin establishes a voltage drop across the external resistor that represents the drain-to-source voltage across the top side N-channel MOSFET during an over current condition. The ILIM over current comparator is blanked for the first 100 ns to allow full enhancement of the top MOSFET. Set the ILIM voltage level such that it is within 800 mV of V_{DD} ; that is, $(V_{DD} - 0.8) \leq I_{LIM} \leq V_{DD}$.
LDRV	6	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET
SS/SD	4	I	Soft-start and overcurrent fault shutdown times are set by charging and discharging a capacitor connected to this pin. A closed loop soft-start occurs when the internal 3- μ A current source charges the external capacitor from 0.17 V to 0.70 V. During the soft-start period, the current sink capability of the TPS40001 and TPS40003 is disabled. When the SS/SD voltage is less than 0.12 V, the device is shutdown and the HDRV and LDRV are driven low. In normal operation, the capacitor is charged to 1.5 V. When a fault condition is asserted, the HDRV is driven low, and the LDRV is driven high. The soft-start capacitor goes through six charge/discharge cycles, restarting the converter on the seventh cycle.
SW	8	O	Connect to the switched node on the converter. This pin is used for overcurrent sensing in the topside N-channel MOSFET, zero current sensing in synchronous rectifier N-channel MOSFET, and level sensing for predictive delay circuit. Overcurrent is determined, when the topside N-channel MOSFET is on, by comparing the voltage on SW with respect to VDD and the voltage on the ILIM with respect to VDD. Zero current is sensed, when the rectifier N-channel MOSFET is on, by measuring the voltage on SW with respect to ground. Zero current sensing applies to the TPS40000/2 devices only.
VDD	7	I	Power input for the chip, 5.5-V maximum. Decouple close to the pin with a low-ESR capacitor, 1- μ F or larger.

functional block diagram



UDG-01142

APPLICATION INFORMATION

The TPS4000x series of synchronous buck controller devices is optimized for high-efficiency dc-to-dc conversion in non-isolated distributed power systems. A typical application circuit is shown in Figure 1.

The TPS40004 and TPS40005 are the controllers of choice for most general purpose synchronous buck designs. Each operates in two quadrant mode (i.e. source or sink current) full time. This choice provides the best performance for output voltage load transient response over the widest load current range.

The TPS40001 and TPS40003 add an additional feature: They operate in single quadrant mode (i.e. source current only) during converter startup, and then when the converter has reached the regulation point, the controllers change to operate in two quadrant mode. This is useful for applications that have outputs pre-biased at some voltage before the controller is enabled. When the TPS40001 or TPS40003 is enabled, it does not sink current during startup and therefore does not pull current from the pre-biased voltage supply.

The TPS40000 and TPS40002 operate in single quadrant mode (source current only) full time, allowing the paralleling of converters. Single quadrant operation ensures one converter does not pull current from a paralleled converter. A converter using one of these controllers emulates a non-synchronous buck converter at light loads. When current in the output inductor attempts to reverse, an internal zero-current detection circuit turns OFF the synchronous rectifier and causes the current flow in the inductor to become discontinuous. At average load currents greater than the peak amplitude of the inductor ripple current, the converter returns to operation as a synchronous buck converter to maximize efficiency.

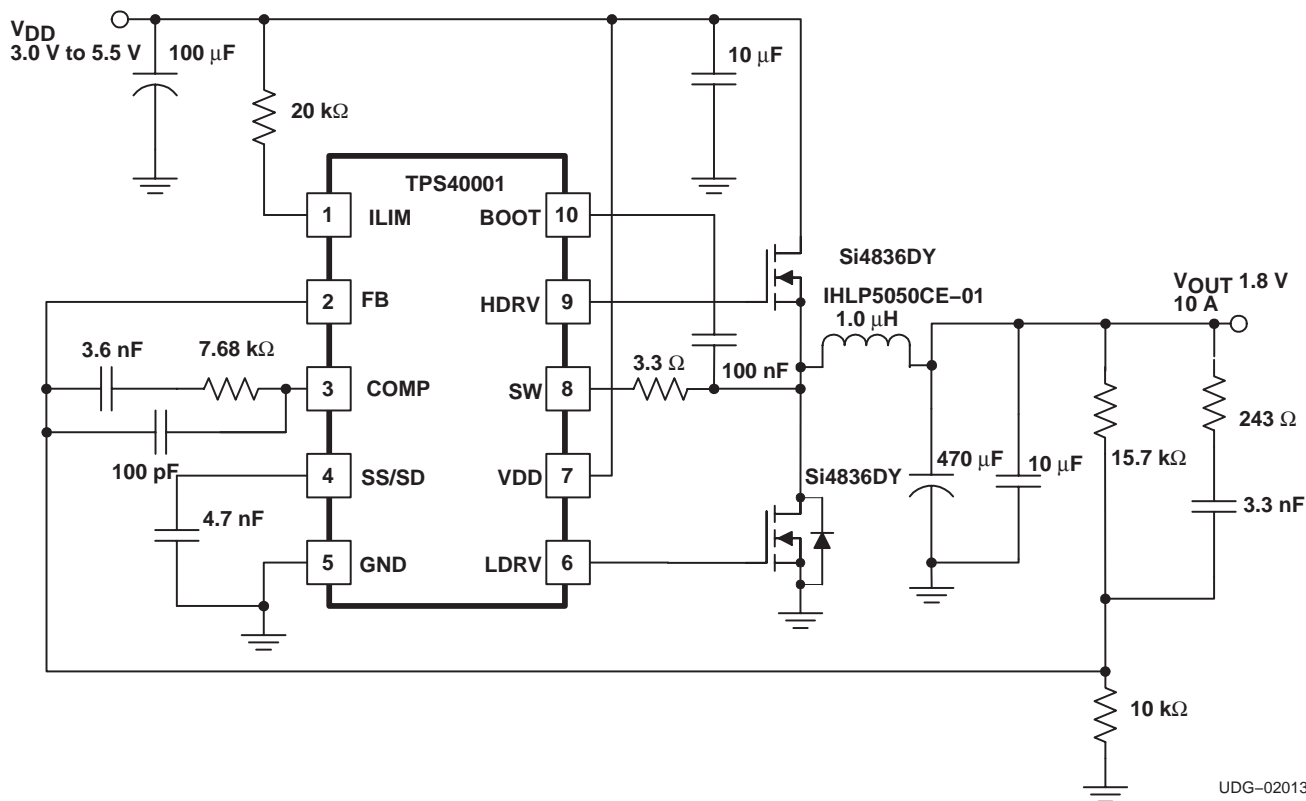


Figure 1. Typical Application Circuit

UDG-02013

APPLICATION INFORMATION

error amplifier

The error amplifier has a bandwidth of greater than 5 MHz, with open loop gain of at least 55 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large-scale transient response.

oscillator

The oscillator uses an internal resistor and capacitor to set the oscillation frequency. The ramp waveform is a triangle at the PWM frequency with a peak voltage of 1.25 V, and a valley of 0.25 V. The PWM duty cycle is limited to a maximum of 95%, allowing the bootstrap capacitor to charge during every cycle.

bootstrap/charge pump

There is an internal switch between VDD and BOOT. This switch charges the external bootstrap capacitor for the floating supply. If the resistance of this switch is too high for the application, an external schottky diode between VDD and BOOT can be used. The peak voltage on the bootstrap capacitor is approximately equal to VDD.

driver

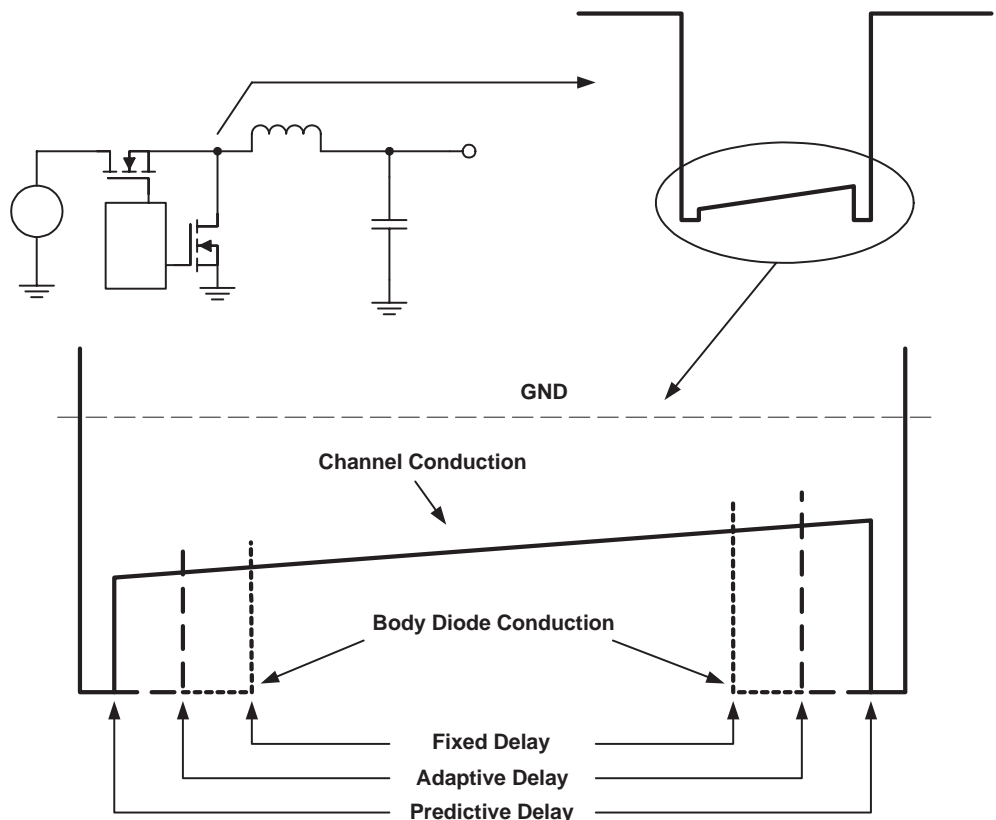
The HDRV and LDRV MOSFET drivers are capable of driving gate-to-source voltages up to 5.5 V. At $V_{IN} = 5$ V and using appropriate MOSFETs, a 20-A converter can be achieved. The LDRV driver switches between VDD and ground, while the HDRV driver is referenced to SW and switches between BOOT and SW. The maximum voltage between BOOT and SW is 5.5 V.

synchronous rectification and predictive delay

In a normal buck converter, when the main switch turns off, current is flowing to the load in the inductor. This current cannot be stopped immediately without using infinite voltage. For the current path to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a conventional diode, or it can be a controlled active device if a control signal is available to drive it. The TPS4000x provides a signal to drive an N-channel MOSFET as a rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is minimum delay from the time that the rectifier MOSFET turns off and the main switch turns on, and minimum delay from when the main switch turns off and the rectifier MOSFET turns on. This scheme, Predictive Gate Drive™ delay, uses information from the current switching cycle to adjust the delays that are to be used in the next cycle. Figure 2 shows the switch-node voltage waveform for a synchronously rectified buck converter. Illustrated are the relative effects of a fixed-delay drive scheme (constant, pre-set delays for the turn-off to turn-on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme.

Note that the longer the time spent in diode conduction during the rectifier conduction period, the lower the efficiency. Also, not described in Figure 2 is the fact that the predictive delay circuit can prevent the body diode from becoming forward biased at all while at the same time avoiding cross conduction or shoot through. This results in a significant power savings when the main MOSFET turns on, and minimizes reverse recovery loss in the body diode of the rectifier MOSFET.

APPLICATION INFORMATION



UDG-01144

Figure 2. Switch Node Waveforms for Synchronous Buck Converter

overcurrent

Overcurrent conditions in the TPS4000x are sensed by detecting the voltage across the main MOSFET while it is on.

basic description

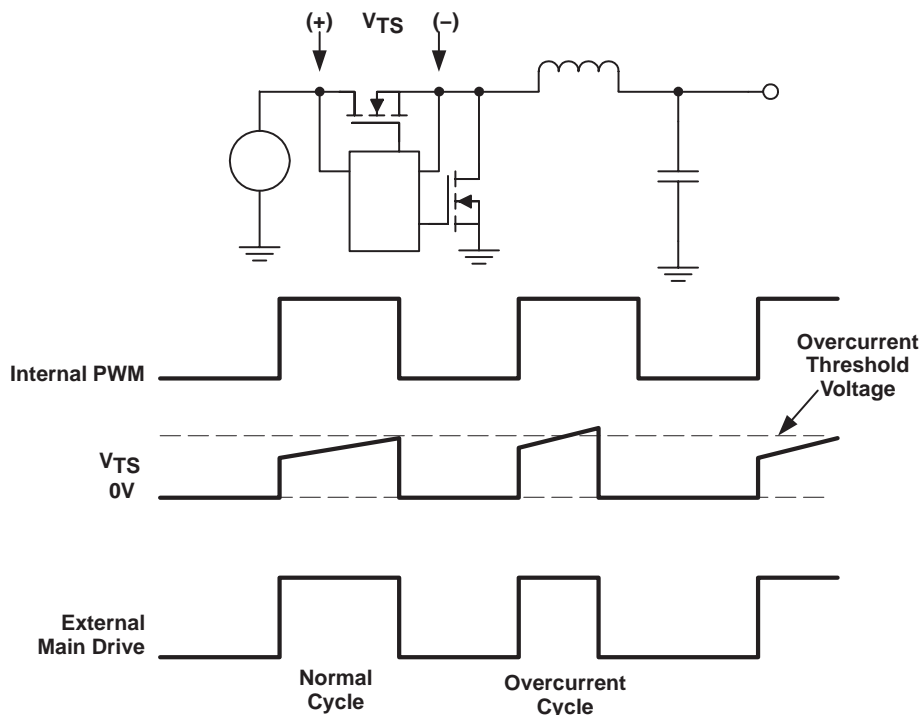
If the voltage exceeds a pre-set threshold, the current pulse is terminated, and a counter inside the device is incremented. If this counter fills up, a fault condition is declared and the device disables switching for a period of time and then attempts to restart the converter with a full soft-start cycle.

APPLICATION INFORMATION

detailed description

During each switching cycle, a comparator looks at the voltage across the top side MOSFET while it is on. This comparator is enabled after the SW node reaches a voltage greater than $(V_{DD}-1.2\text{ V})$ followed by a 100-ns blanking time. If the voltage across that MOSFET exceeds a programmable threshold voltage, the current-switching pulse is terminated and a 3-bit counter is incremented by one count. If, during the switching cycle, the topside MOSFET voltage does not exceed a preset threshold, then this counter is decremented by one count. (The counter does not wrap around from 7 to 0 or from 0 to 7). If the counter reaches a full count of 7, the device declares that a fault condition exists at the output of the converter. In this fault state, HDRV is turned off and LDRV is turned on and the soft-start capacitor is discharged. The counter is decremented by one by the soft start capacitor (C_{SS}) discharge. When the soft-start capacitor is fully discharged, the discharging circuit is turned off and the capacitor is allowed to charge up at the nominal charging rate. When the soft-start capacitor reaches about 700 mV, it is discharged again and the overcurrent counter is decremented by one count. The capacitor is charged and discharged, and the counter decremented until the count reaches zero (a total of six times). When this happens, the outputs are again enabled as the soft-start capacitor generates a reference ramp for the converter to follow while attempting to restart.

During this soft-start interval (whether or not the controller is attempting to do a fault recovery or starting for the first time), pulse-by-pulse current limiting is in effect, but overcurrent pulses are not counted to declare a fault until the soft-start cycle has been completed. It is possible to have a supply attempt to bring up a short circuit for the duration of the soft start period plus seven switching cycles. Power stage designs should take this into account if it makes a difference thermally. Figure 3 shows the details of the overcurrent operation.

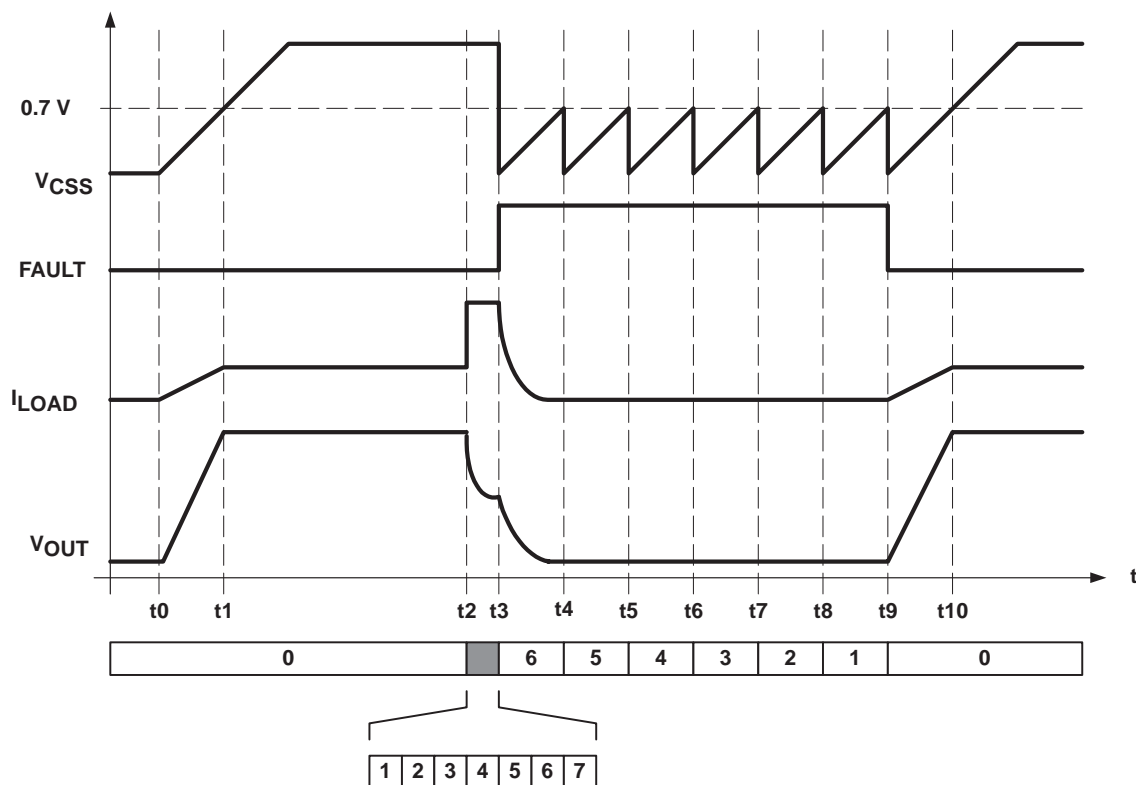


UDG-01145

Figure 3. Switch Node Waveforms for Synchronous Buck Converter

APPLICATION INFORMATION

Figure 4 shows the behavior of key signals during initial startup, during a fault and a successfully fault recovery. At time t_0 , power is applied to the converter. The voltage on the soft-start capacitor (V_{CSS}) begins to ramp up and acts as the reference until it passes the internal reference voltage at t_1 . At this point the soft-start period is over and the converter is regulating its output at the desired voltage level. From t_0 to t_1 , pulse-by-pulse current limiting is in effect, and from t_1 onward, overcurrent pulses are counted for purposes of determining a possible fault condition. At t_2 , a heavy overload is applied to the converter. This overload is in excess of the overcurrent threshold. The converter starts limiting current and the output voltage falls to some level depending on the overload applied. During the period from t_2 to t_3 , the counter is counting overcurrent pulses, and at time t_3 reaches a full count of 7. The soft-start capacitor is then discharged, the counter is decremented, and a fault condition is declared. At t_4 , the overload is removed. The counter continues to count down from 6 to 0. At t_9 , the counter reaches 0. The fault logic is then cleared, the outputs are enabled, and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at t_{10} .



UDG-01144

Figure 4. Switch Node Waveforms for Synchronous Buck Converter

When the soft start capacitor is fully discharged, it begins charging again at the same rate that it does on startup, with a nominal 3- μ A current source. As the capacitor voltage reaches full charge, it is discharged again and the counter is decremented by one count. These transitions occur at t_3 through t_9 . At t_9 , the counter has been decremented to 0. The fault logic is then cleared, the outputs are enabled, and the converter attempts to restart with a full soft-start cycle. The converter comes into regulation at t_{10} .

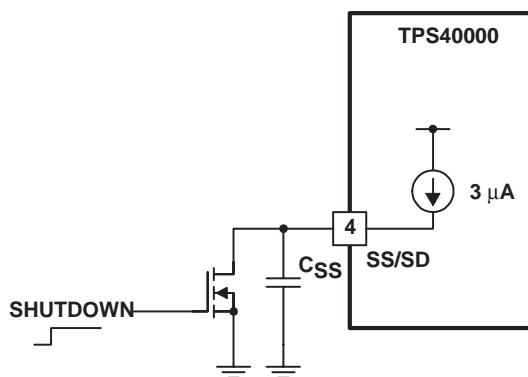
APPLICATION INFORMATION

setting the current limit

Connecting a resistor from VDD to ILIM sets the current limit. A 15- μ A current sink internal to the device causes a voltage drop at ILIM that is equal to the overcurrent threshold voltage. Ensure that $(V_{DD}-0.8\text{ V}) \leq V_{ILIM} \leq V_{DD}$. The tolerance of the current sink is too loose to do an accurate current limit. The main purpose is for hard fault protection of the power switches. Given the tolerance of the ILIM sink current, and the $R_{DS(on)}$ range for a MOSFET, it is generally possible to apply a load that thermally damages the converter. This device is intended for embedded converters where load characteristics are defined and can be controlled.

soft-start and shutdown

These two functions are common to the SS/SD pin. The voltage at this pin is the controlling voltage of the error amplifier during startup. This reduces the transient current required to charge the output capacitor at startup, and allows for a smooth startup with no overshoot of the output voltage if done properly. A shutdown feature can be implemented as shown in Figure 5.



UDG-01143

Figure 5. Shutdown Implementation

The device shuts down when the voltage at the SS/SD pin falls below 120 mV. Because of this limitation, it is recommended that a MOSFET be used as the controlling device, as in Figure 5. An open-drain CMOS logic output would work equally well.

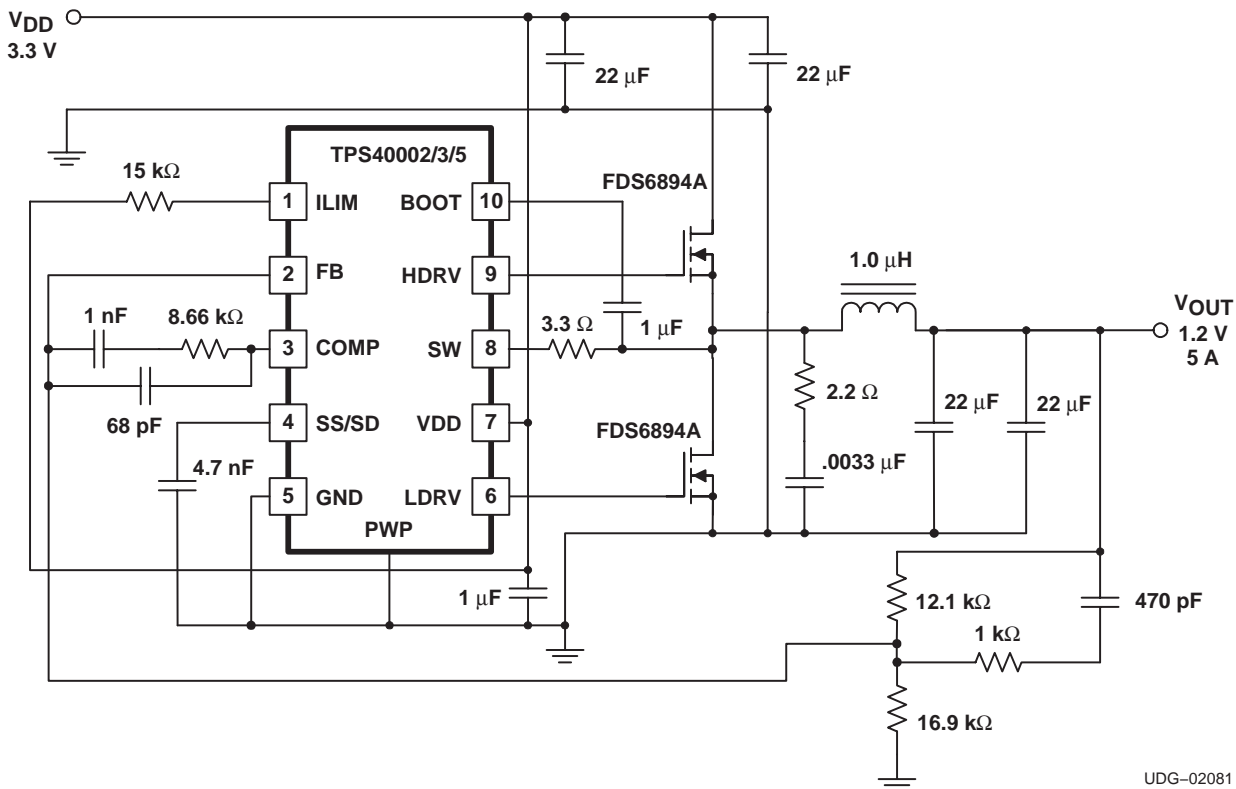
rectifier zero-current

Both the TPS40000 and TPS40002 parts are source-only, thus preventing reverse current in the synchronous rectifier. Synchronous rectification is terminated by sensing the voltage, SW with respect to ground, across the low-side MOSFET. When SW node is greater than -7 mV , rectification is terminated and stays off until the next PWM cycle. In order to filter out undesired noise on the SW node, the zero-current comparator is blanked for 75 ns from the time the rectifier is turned on.

The TPS40001 and TPS40003 parts enable the zero-current comparator, (and therefore prevent reverse current), while soft-start is active. However, when the output reaches regulation; that is, at the end of the soft-start time, this comparator is disabled to allow the synchronous rectifier to sink current.

APPLICATION INFORMATION

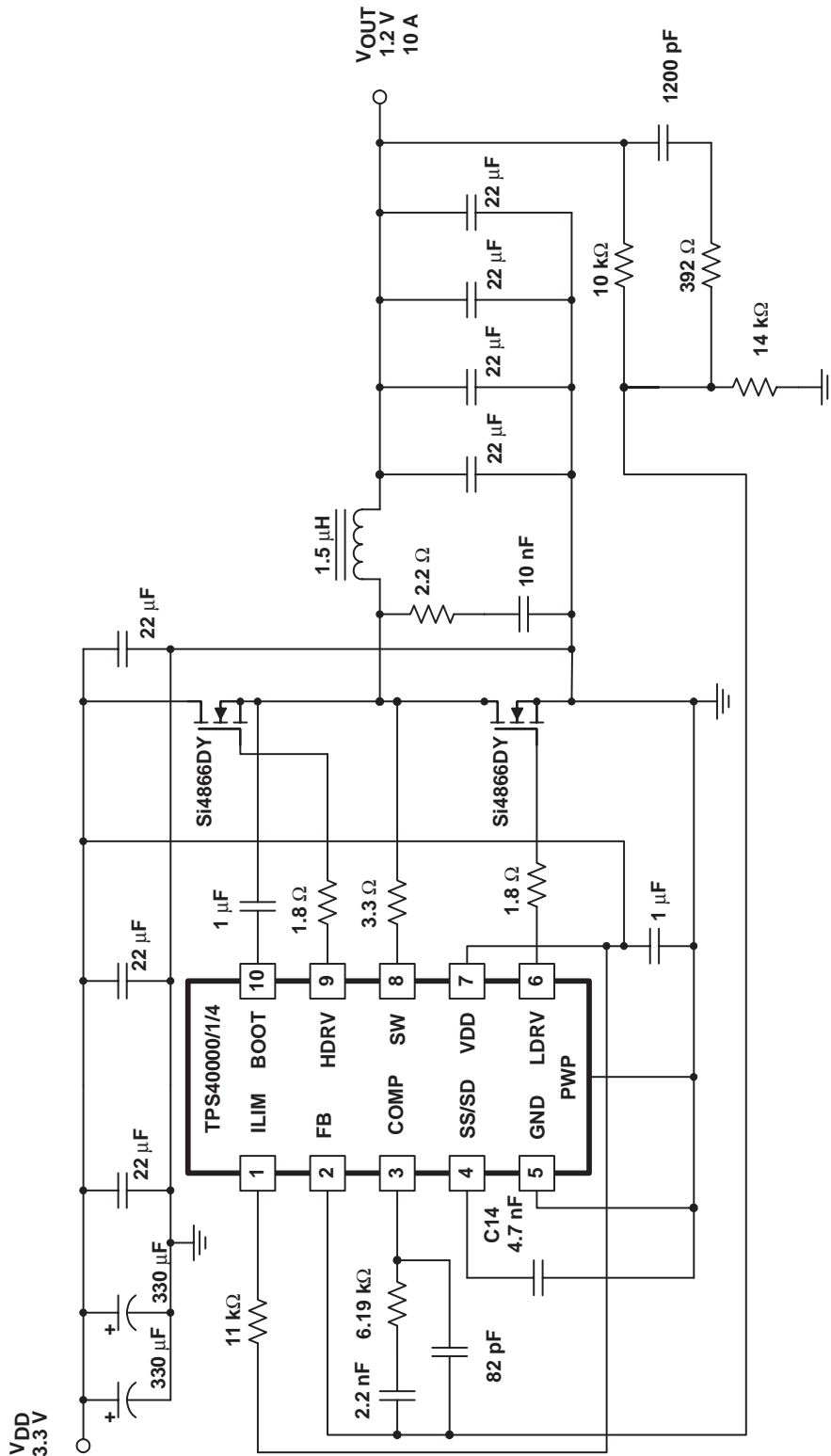
The following pages include design ideas for a few applications. For more ideas, detailed design information, and helpful hints, visit the TPS40000 resources at <http://power.ti.com>.



UDG-02081

Figure 6. Small-Form Factor Converter for 3.3 V to 1.2 V at 5 A.

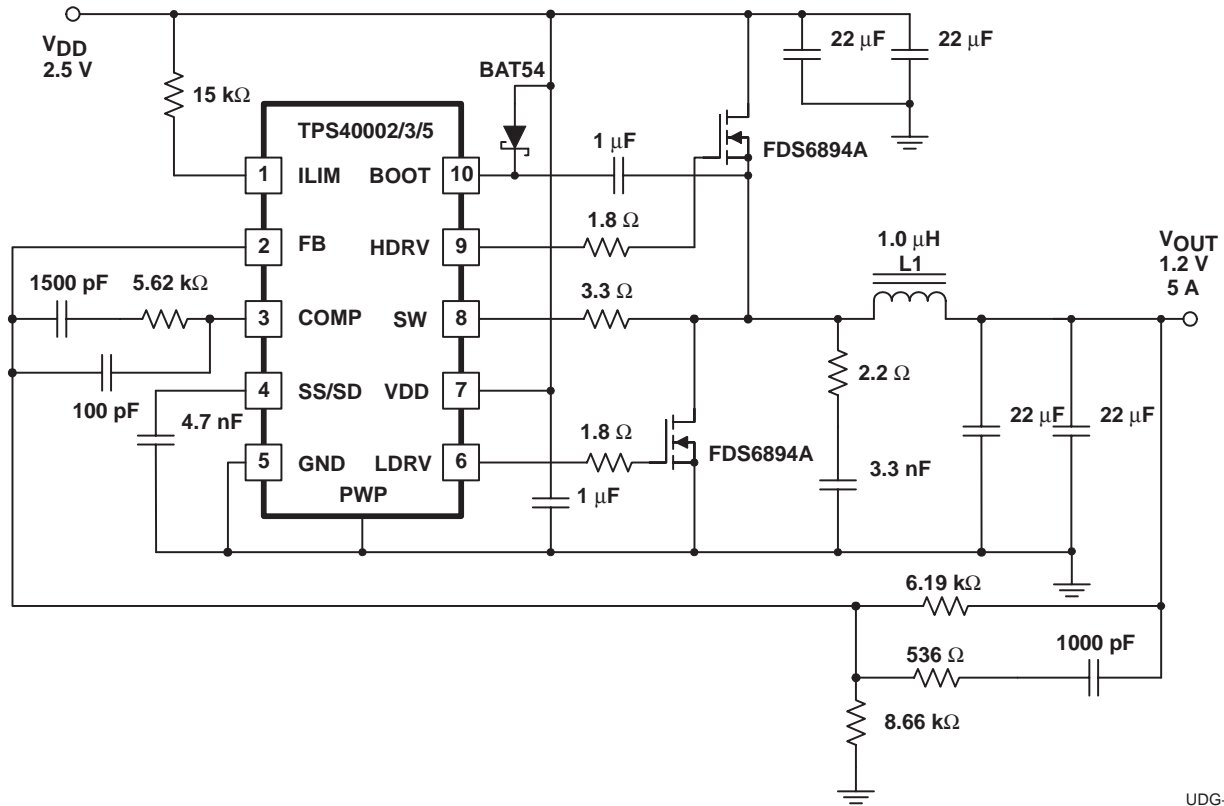
APPLICATION INFORMATION



UDG-02082

Figure 7. High-Current Converter for 3.3 V to 1.2 V at 10 A.

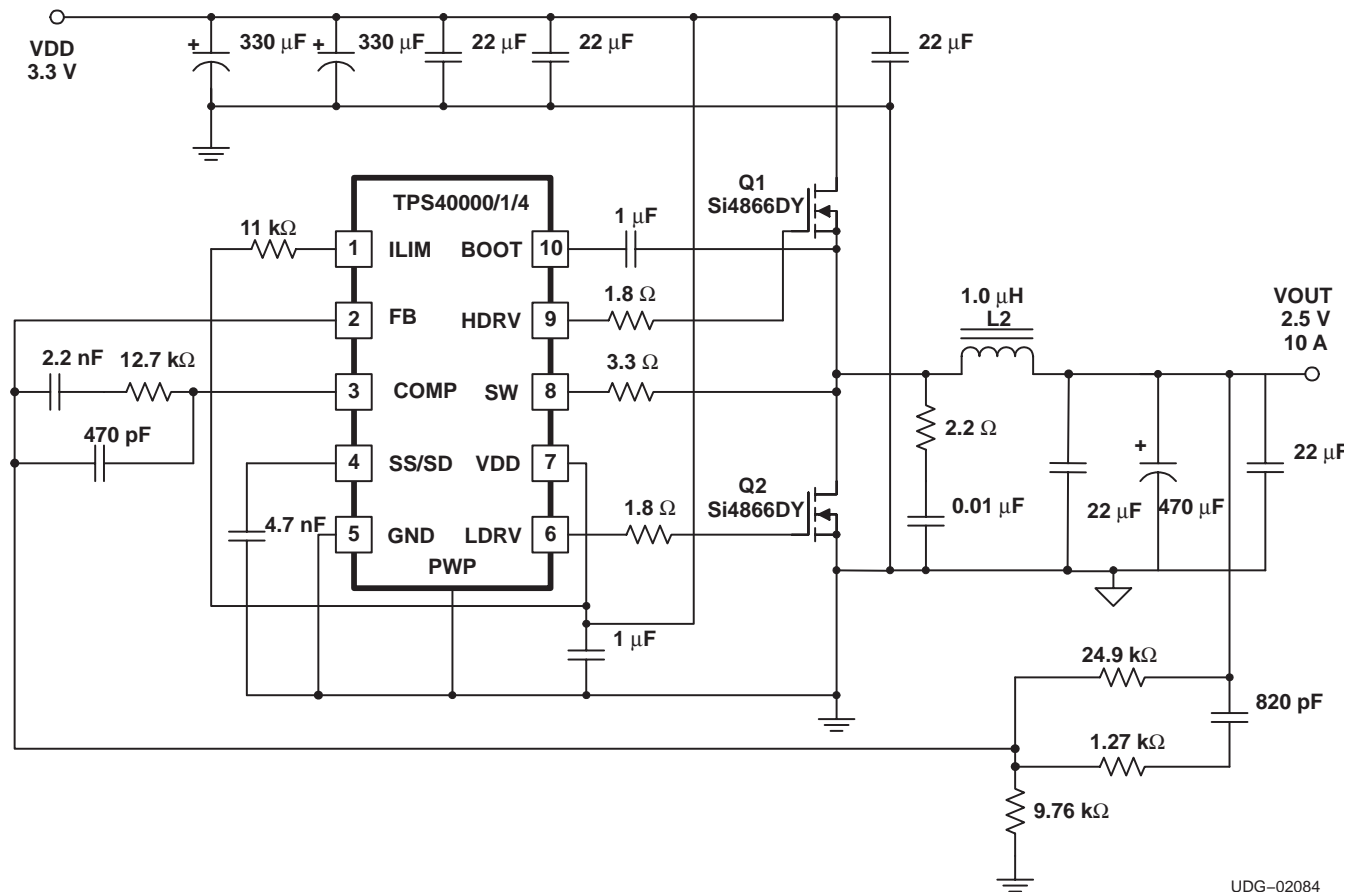
APPLICATION INFORMATION



UDG-02083

Figure 8. Ultra-Low-Input Voltage Converter for 2.5 V to 1.2 V at 5 A

APPLICATION INFORMATION



UDG-02084

Figure 9. Ultra-High-Efficiency Converter for 3.3 V to 2.5 V at 10 A

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY PERCENT CHANGE
 VS
 INPUT VOLTAGE

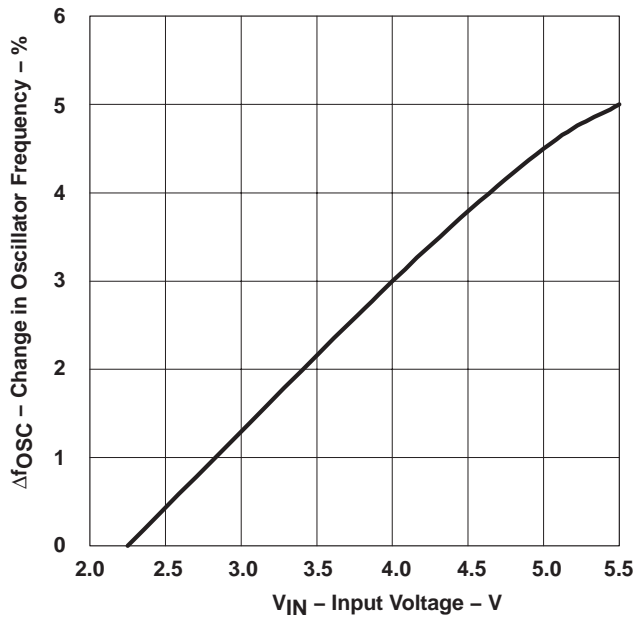


Figure 10

OSCILLATOR FREQUENCY PERCENT CHANGE
 VS
 TEMPERATURE

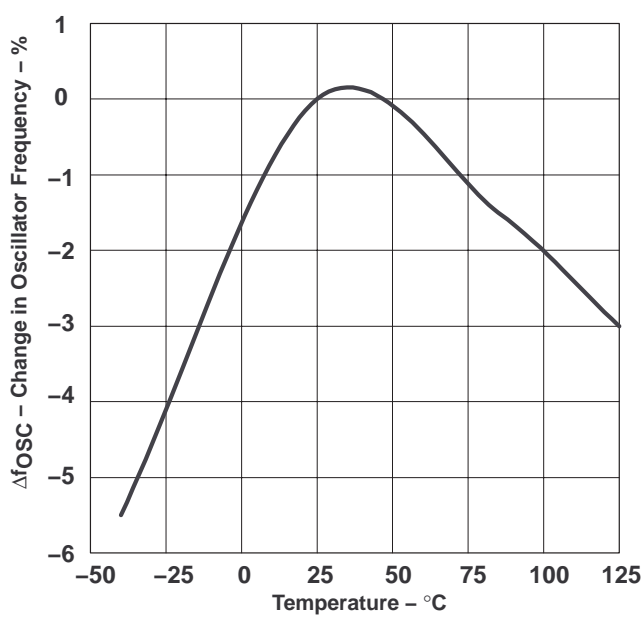


Figure 11

FEEDBACK VOLTAGE
 VS
 INPUT VOLTAGE

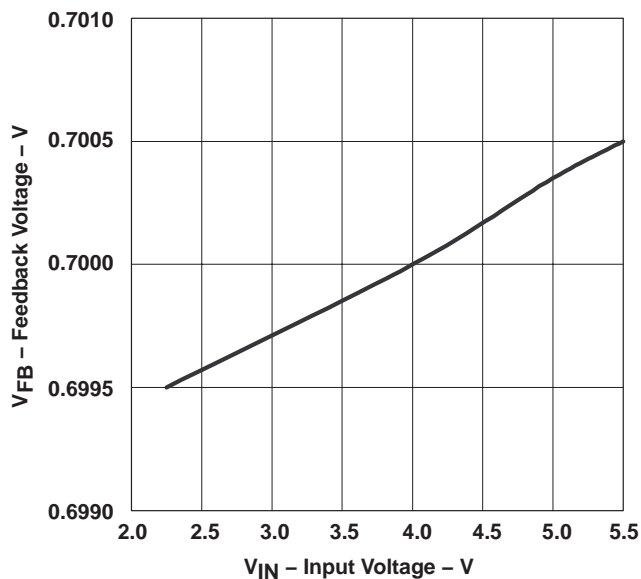


Figure 12

FEEDBACK VOLTAGE
 VS
 TEMPERATURE

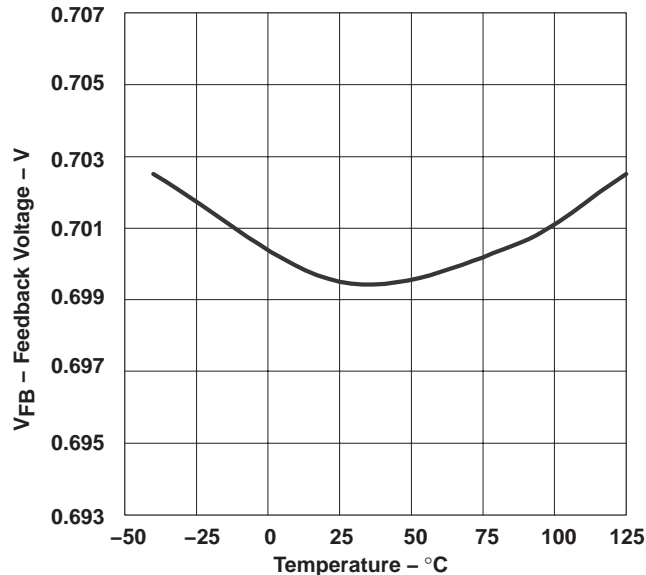
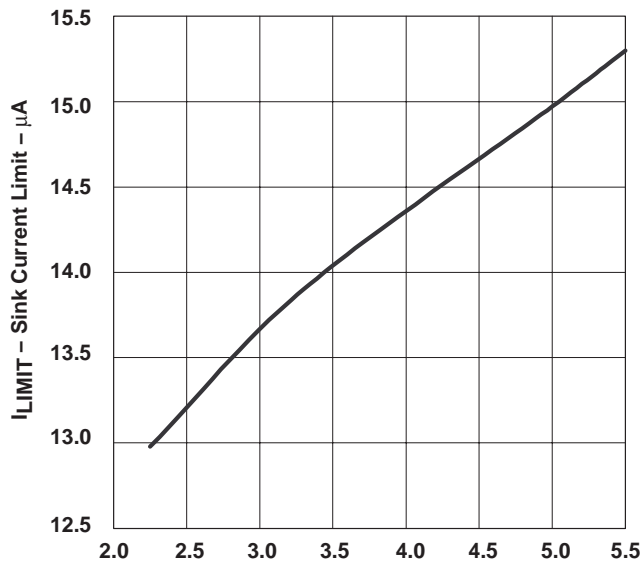


Figure 13

TYPICAL CHARACTERISTICS

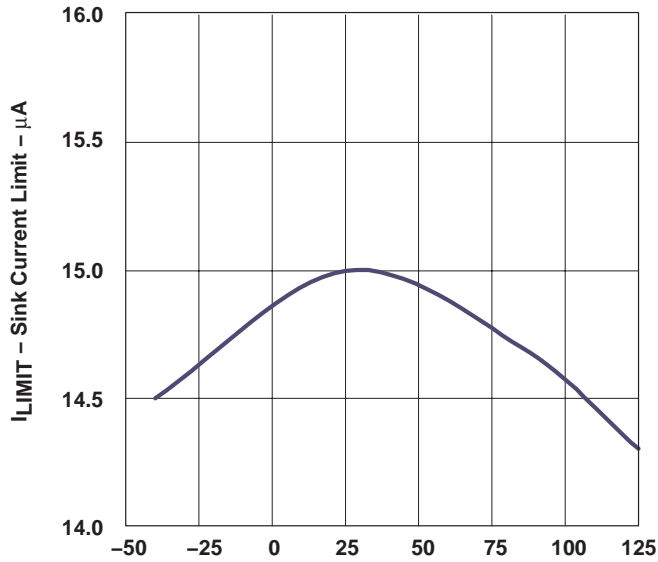
CURRENT LIMIT SINK CURRENT
 vs
 INPUT VOLTAGE



V_{IN} - Input Voltage - V

Figure 14

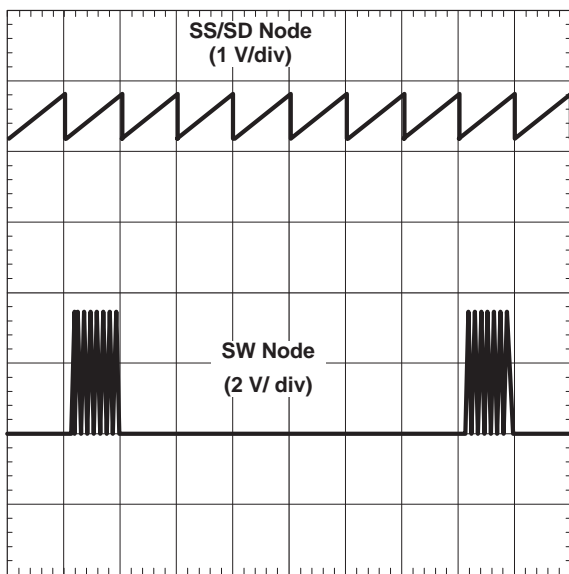
CURRENT LIMIT SINK CURRENT
 vs
 TEMPERATURE



Temperature - °C

Figure 15

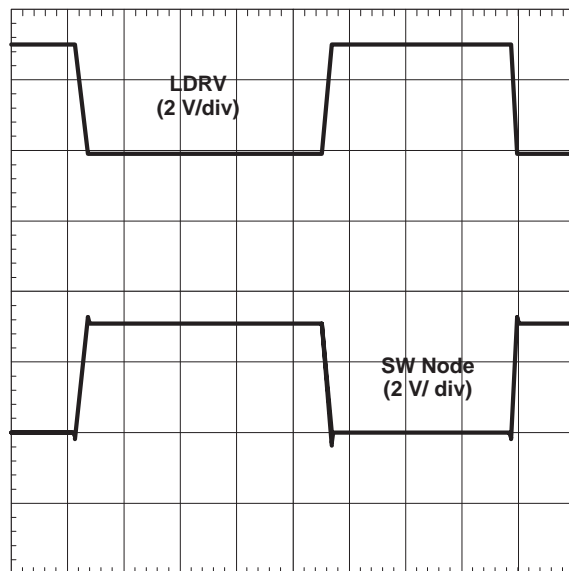
OVERCURRENT



t - Time - 1 ms/div

Figure 16

TYPICAL PREDICTIVE
 DELAY SWITCHING



t - Time - 400 ns/div

Figure 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40000DGQ	ACTIVE	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40000DGQG4	ACTIVE	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40000DGQR	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	40000	Samples
TPS40001DGQ	NRND	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40001	
TPS40001DGQR	NRND	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40001	
TPS40001DGQRG4	NRND	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40001	
TPS40002DGQ	NRND	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40002	
TPS40002DGQR	NRND	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40002	
TPS40003DGQ	NRND	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40003	
TPS40003DGQG4	NRND	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40003	
TPS40003DGQR	NRND	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40003	
TPS40005DGQR	NRND	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40005	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40000DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40001DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40002DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40003DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS40005DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

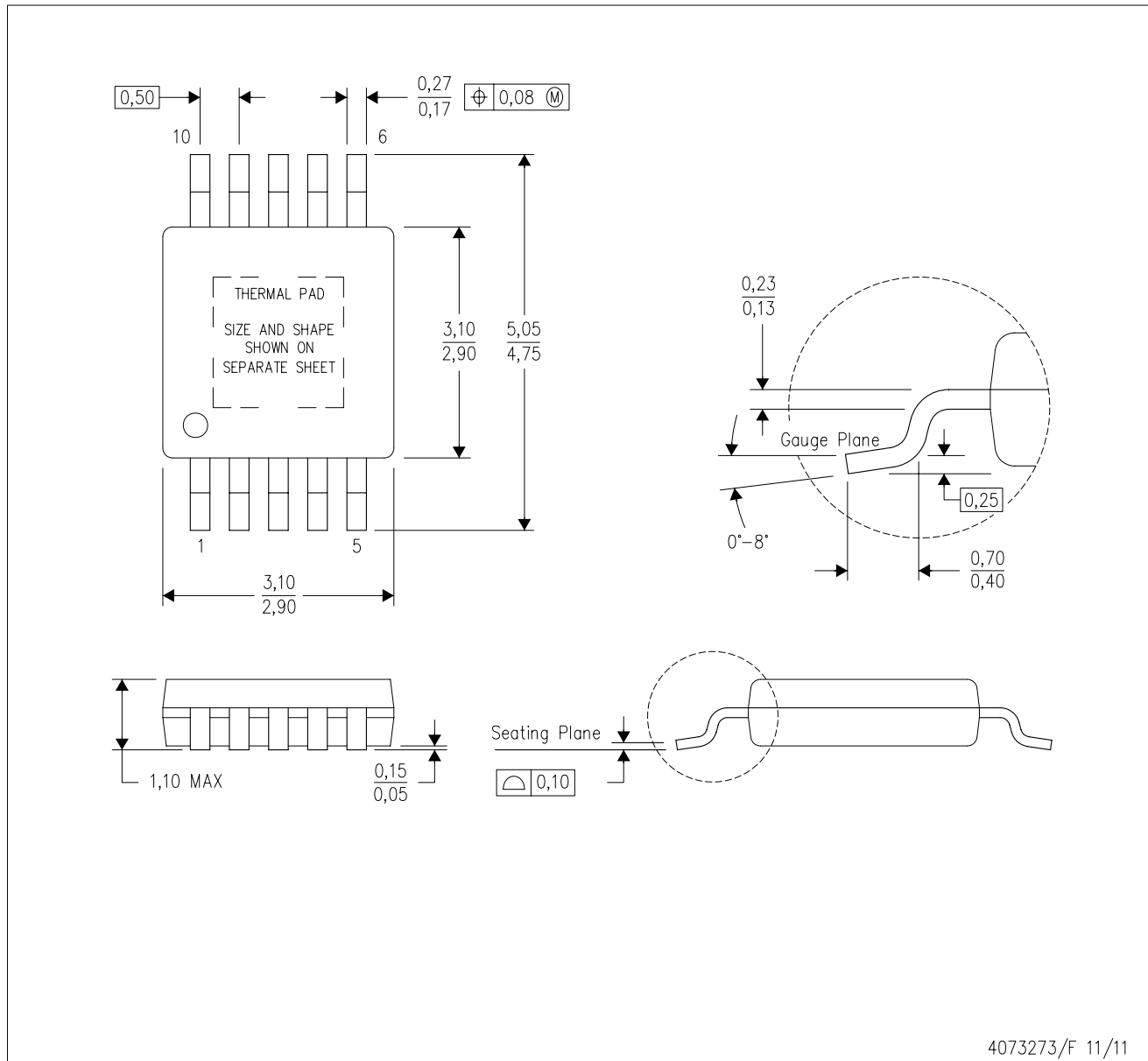
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS4000DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
TPS4001DGQR	HVSSOP	DGQ	10	2500	370.0	355.0	55.0
TPS4002DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0
TPS4003DGQR	HVSSOP	DGQ	10	2500	370.0	355.0	55.0
TPS4005DGQR	HVSSOP	DGQ	10	2500	346.0	346.0	35.0

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

DGQ (S-PDSO-G10)

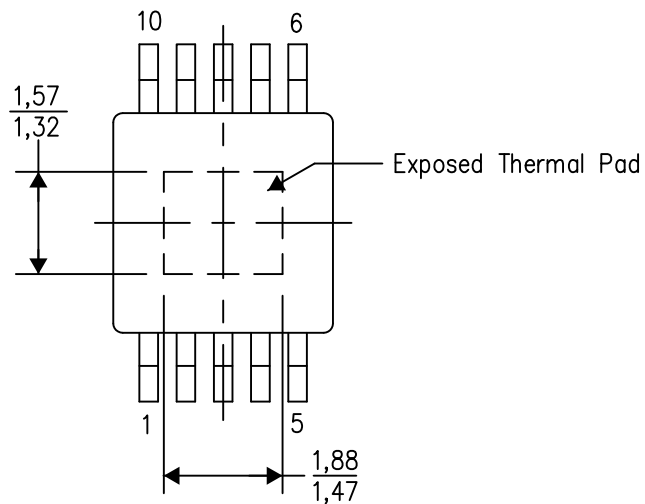
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



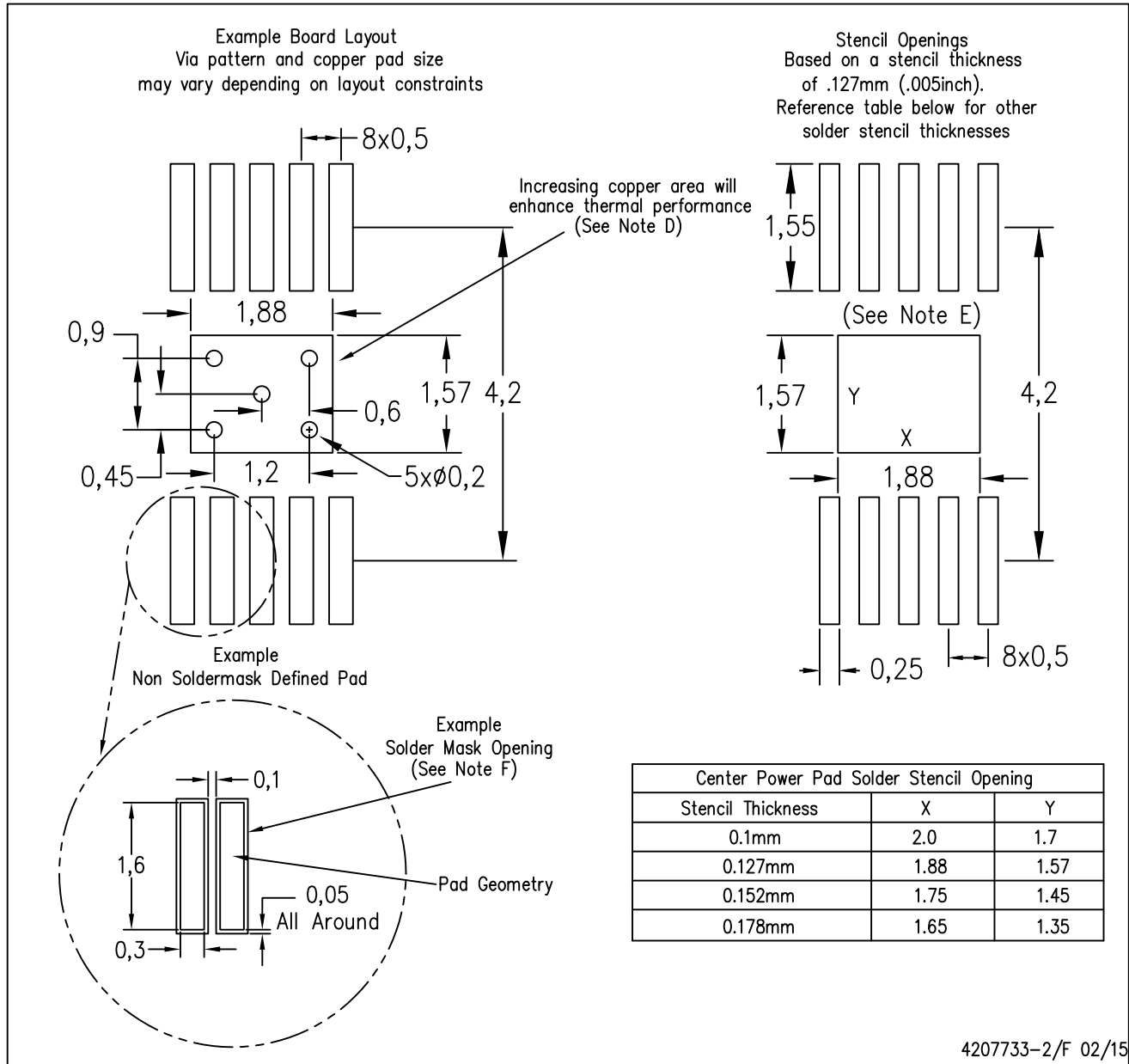
Top View

Exposed Thermal Pad Dimensions

4206324-2/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DGQ (S-PDSO-G10)

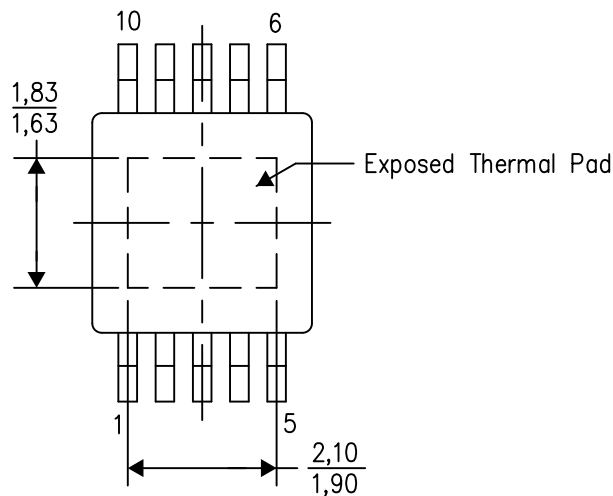
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206324-6/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated